ABSTRACT OF THE DISCLOSURE

Methods for calculating delays for cells in ASICs are disclosed. In the present invention, delays are computed by considering not only the process (P), voltage (V), temperature (T) but also input ramptime (R) and output load or fanout (F) of the cells by fitting the delay at four corner points for derated PVT condition into a non-linear equation which is a function of P, V, T, R and F. Thus, the delay is a five dimensional characterization, and the characterization is split into (P,V,T) characterization and (R,T) characterization to reduce the characterization time and resources. The present invention provides for accurate calculation of delays for cells in ASICs.